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DIGITAL FM MODULATOR AND DEMODULATOR FOR SDR

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ABSTRACT

This paper deals with an FPGA implementation of a high performance FM modulator and demodulator for software defined Radio (SDR) system. The individual component of proposed FM modulator and demodulator has been optimized in such a way that the overall design consists of a high-speed, area optimized and low-power features. The modulator and demodulator contain An optimized direct digital frequency synthesizer (DDFS) based on quarter-wave symmetry technique for generating the carrier Frequency with spurious free dynamic range (SFDR) of more than 64 DB. The FM modulator uses pipelined version of the DDFS to Support the up conversion in the digital domain. The proposed FM modulator and demodulator can operate at a maximum frequency of 334.5MHz and 131MHz involving around 1.93 K and 6.4 K equivalent gates for FM modulator and FM demodulator respectively. After applying a 10 KHz triangular wave input and by setting the system clock frequency to 100MHz using Xpower the power has been calculated. The FM modulator consumes 107.67mW power while FM demodulator consumes 108.67mW power for the same input running at same data rate.

KEYWORDS: Field Programmable gate array(FPGA), Software defined Radio(SDR) Direct Digital Frequency Synthesizer (DDFS), Spurious Free Dynamic Range (SFDR).

INTRODUCTION

Baseband signal processing technology is experiencing a period of radical change for both handset and base station application with 3G, emerging as the major river. This emerging technology has evolved towards the concept of software defined radio rather than the previous analog hardware defined radio. SDR uses programmable digital Devices to perform the signal processing necessary to transmit and receive the baseband information at radio frequency. Recent mobile handset must have the various communication protocol support to connect anywhere and anytime for the user end. Devices such as digital signal processors (DSPs) and field programmable gate array (PGAs) use software to incorporate them with the required signal processing functionality. This technology offers greater flexibility and potentially longer product life, since the radio can be upgraded very cost efficiently with software. In presence of different communication protocol the software will configure the hardware over the air according to the needs. Frequency modulation/demodulation scheme is widely used for supporting the DAB-T and private mobile radio (PMR) standards amongst others. Audio or voice clarity is the main concern in any audio broadcasting standards. Using the VCO it is very difficult to obtain a good clarity in the FM modulated or demodulated signal as VCO suffers from lack of linearity over the desired frequency range. This has paved the way for digital implementation of FM modulation scheme which has evolved to replace the analog counterpart to ensure linearity over the entire frequency range, designers choose to replace the VCO by a DDS, sometimes referred as numerically controlled oscillator (NCO).

FM MODULATOR AND FM DEMODULATOR

FM MODULATOR:

FM is a type of angle modulation where instantaneous frequency of the carrier signal varies linearly with the baseband modulated signal m (t) as follows

$$S_{FM}(t) = A_c \cos\left[2\pi F_c t + 2\pi K_f \int m(n)dn\right]$$

Where Ac is the amplitude of the carrier, Fc is the carrier frequency and Kf is the frequency deviation constant. The FM modulator consists of an adder and a DDS block. The adder block adds the instantaneous frequency of the input

message signal to the carrier frequency. And finally DDS block take this frequency as an input and generates the FM modulated signal. The architecture of the DDS block has been discussed in the later section. The mean-square power spectral density spectrum of the designed FM modulator has been shown in Figure 1.

Figure

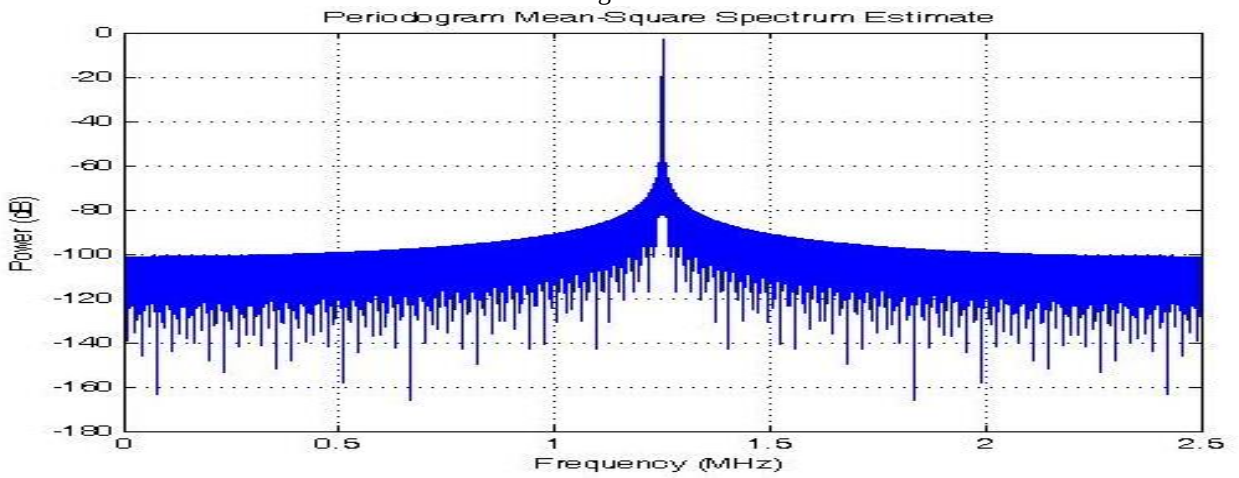

Figure 1 Mean square power spectral density spectrogram of FM modulator

FM DEMODULATOR:

Operation of the digital phase locked loop as a demodulator has been conceived in the early 1970s [13-14] and as a near optimum FM receiver. The complete FM receiver consists of the basic building blocks as shown in Figure 2. The FM receiver consists of four basic parts: (A) Phase Detector (B) Loop Filter (C) Direct Digital Synthesizer (D) FIR Filter.

Output of the phase detector is the product of these two signals. Using familiar trigonometric identity, it is found as

$$V_d(t)=K_d[V_{i(t)} * V_{0(t)}]$$

$$V_d(t)=K_d\left[\sin(\omega_i t+\theta_0(t)).\cos(\omega_i t+\theta_0(t)).\right]$$

$$=\frac{K_d}{}\left[\sin(2\omega_i t+\theta_i(t)+\theta_0(t))+\sin(\theta_i(t)-\theta_0(t))\right]$$

Where K_d is the gain of the phase detector, $V_{i(t)}$ is the frequency modulated signal and $V_{0(t)}$ is the sinusoidal signal generated from the DDS. The first term in (2) corresponds to high frequency component. The second term corresponds to the phase difference between $V_{i(t)}$ and $V_{0(t)}$. The phase difference between the modulated signal and the carrier ($\theta_i(t)$ - $\theta_0(t)$ produces the desired original signal.

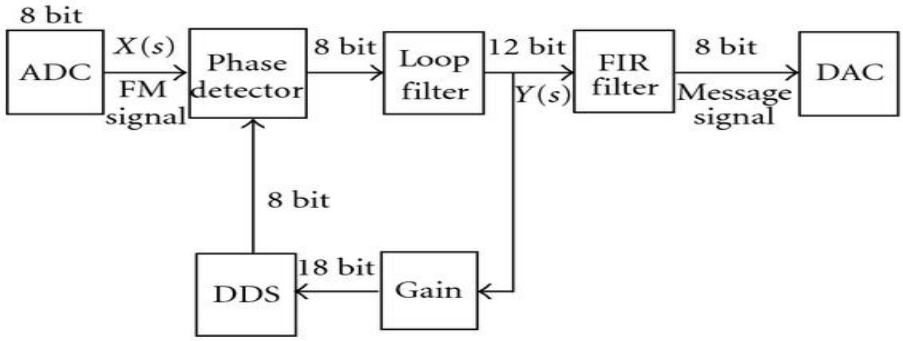

Figure 2. Block Diagram of Digital FM Receiver Circuit

The transfer function of the system is

$$\frac{Y(s)}{X(s)} = \frac{-s^2 + s}{1.3375s^2 + 0.06161s + 0.00089}$$

The second order DPLL system improves the performance of the loop in terms of speed and locking range as compared with a first order DPLL system.

PHASE DETECTOR

The task of the phase detector is to detect the phase error between the incoming frequency modulated signal from the ADC and the output frequency generated from the DDS. This operation needs one register and one multiplier module. The modified Booth Encoded Wallace-tree multiplier [15-16] architecture is used to implement the multiplier module. This architecture helps to reduce the number of partial products from N to N/2 for multiplying an N-bit operand with an M-bit operand. In addition, Ardekani's sign extension technique has been adopted for signed multiplication.

LOOP FILTER

Loop filter, which is a 1st order low pass filter by its characteristics, is used to remove the high frequency components in (2). The transfer function of the loop filter is

$$H(z) = \frac{1}{z - \alpha}.$$

The equation (4) can be implemented in hardware by the addition of the output signal from the phase detector and the register output multiplied by the coefficient = (1-1/16)=15/16=0.9375, which is chosen to ensure the system stability. The complex multiplication has been done in such a way so that the multiplication operation can be implemented by just 4 bit right shift instead of a multiplier.

DIRECT DIGITAL SYNTHESIZER

DDS will take the corrective error voltage, Vd(t) and then shift its output frequency from its free running value to the input signal frequency i and thus keep the DPLL in lock. A common method for digitally generating a complex or real valued sinusoid employs a look-up table. A digital integrator is used to generate a suitable phase argument that is mapped by the look-up table into the desired output waveform. In the present paper, one look-up table based DDS architecture is used as shown in Figure 3. The DDS has a free running frequency of 1MHz and it requires 1024 values to define one cycle of cosine signal. One cycle can be divided into four quarters. The first quarter is only needed with 256 sample values. To implement DDS, only a 256X8 bit ROM can be used instead of using 1024 X8 bit ROM to store the 1024 values of cosine signal. Depth of look-up table and the data width has been chosen in such a way so that it can meet the minimum spurious free dynamic range (SFDR) of 70dB [18-19]. The input phase will be accumulated in the accumulator and it will go through the quadrant checking. Based on the quadrant, the multiplexer will select the stored COSROM look up table values, in un-complemented form for the first and fourth quarter while the complemented values for the second and third quarter.

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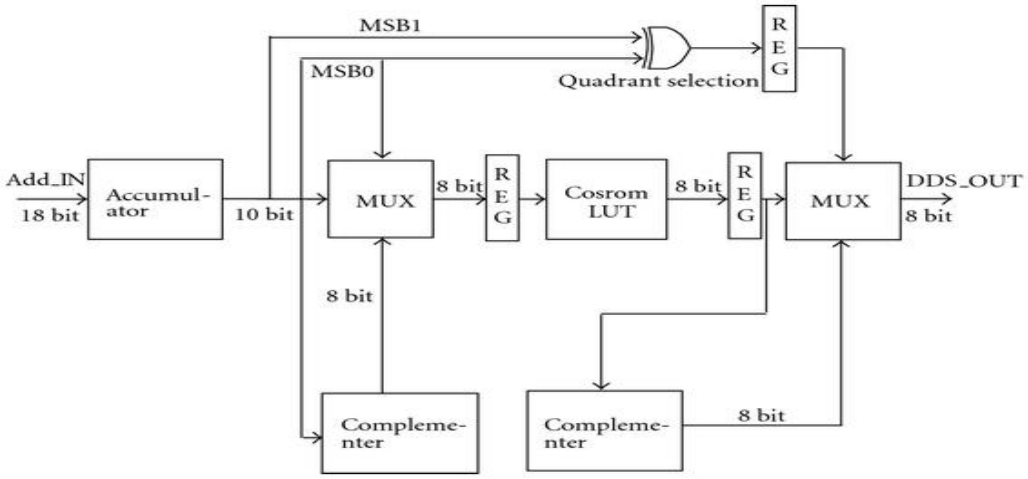

Figure 3. Block Diagram of Direct Digital Synthesizer

FIR FILTER

At the last stage of the receiver, one low pass 16-tap Finite Impulse Response (FIR) filter is used to perform the signal shaping. This filter is essentially an averaging filter since its output is equal to the average value of its input over the last n-tap samples where n is the number of tap used. As in direct form digital FIR filter the total propagation delay of the circuit became more due to the addition of the 16 data samples, here transposed FIR filter architecture is chosen [20-22]. Here the coefficients are the same 1/16, and in reality 1/16 can be implemented by just 4 bit right shift operation. Hence no multiplier is required.

FPGA IMPLEMENTATION DETAILS

Synthesis Results:- The proposed FM demodulator has been described using the Verilog hardware description Table 3: Detailed power analysis results for 2vp30-7ff896. FM modulator FM demodulator Clock power 1.72mW 1.72mW Input power 0.73mW 0.33mW Logic power 0.03mW 1.83mW Output power 2.81mW 11mW Signal power 0.04mW 3.23mW Total power 107.67mW 108.67mW language and Xilinx ISE 9.2i is used for synthesis and FPGA implementation. Xilinx XCV2vp30-7FF896 device has been used as the target device for FPGA implementation, XST has been used as a synthesis tool, and XPower has been used for power calculation. The power is being calculated by simulation-based switching activities of all the signals. The synthesis results for the FM modulator and demodulator have been listed in Table 2. Table 3 listed the detailed dynamic power analysis result by applying a 100 Mbps data rate to the FM modulator and demodulator Table 4 shows the component wise implementation reports.

TABLE 2: Timing, Area, and Power results for 2vp30-7ff896.

	Area				Timing (MHz)	Power (mW)
	No. of slice	No. of FF	No. of LUT	Gate count		
FM modulator	96	90	148	1,931	334.5	107.67
FM demodulator	233	240	436	6,400	131	108.67

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Table 3: Detailed power analysis results for 2vp30-7ff896.

	FM modulator	FM demodulator
Clock power	1.72 mW	1.72 mW
Input power	0.73 mW	0.33 mW
Logic power	0.03 mW	1.83 mW
Output power	2.81 mW	11 mW
Signal power	0.04 mW	3.23 mW
Total power	107.67 mW	108.67 mW

Table 4: Component wise FPGA implementation result.

Module name	Maximum frequency (MHz)	FPGA resources used			Gate count
		Slices	Slice FF	No. of LUTs	
FM data generator	1045.8	7	14	0	139
Interpolator	386	12	11	16	318
Pipelined DDFS	334.5	75	55	120	1,325
Accumulator	335.2	9	18	18	357
Phase detector	131	46	0	71	1,106
Loop filter	221	12	12	23	372
DDFS	155.6	87	25	159	1,371
FIR filter	366.7	97	180	194	3,750

SIMULATION RESULTS

For the post place and route simulation in FPGA, the Modelsim-Xe 6.3c Starter version rom Mentor Graphics is used as a logic simulator. The modulated response of a 10 KHz triangular wave is shown in Figure 15. The demodulated response of the FM-modulated signal isas shown in Figure 16. Carrier frequency has been taken to be 1.5MHz by setting the frequency control word to 512 and the input clock to 100MHz with a modulation index of 10. In Figure 13, the signals from the top represent the input triangular wave (TRIANG INPUT), the frequency control word (FCW) for setting the carrier frequency, and the modulated input data (FM MOD). For the triangular wave the modulated signals from the top are the demodulated output data (FM DEMOD), the modulated input data (FM MOD), the FIR filter output (TRI FIR), the loop filter output data (TRI LOOP), the DDS output data (TRI DDS), and finally for phase detector output (TRI PD) shown in Figure 16. At the initial simulation phase, the demodulated output overshoots since the phase synchronization is in convergence phase and after that the system is stable.

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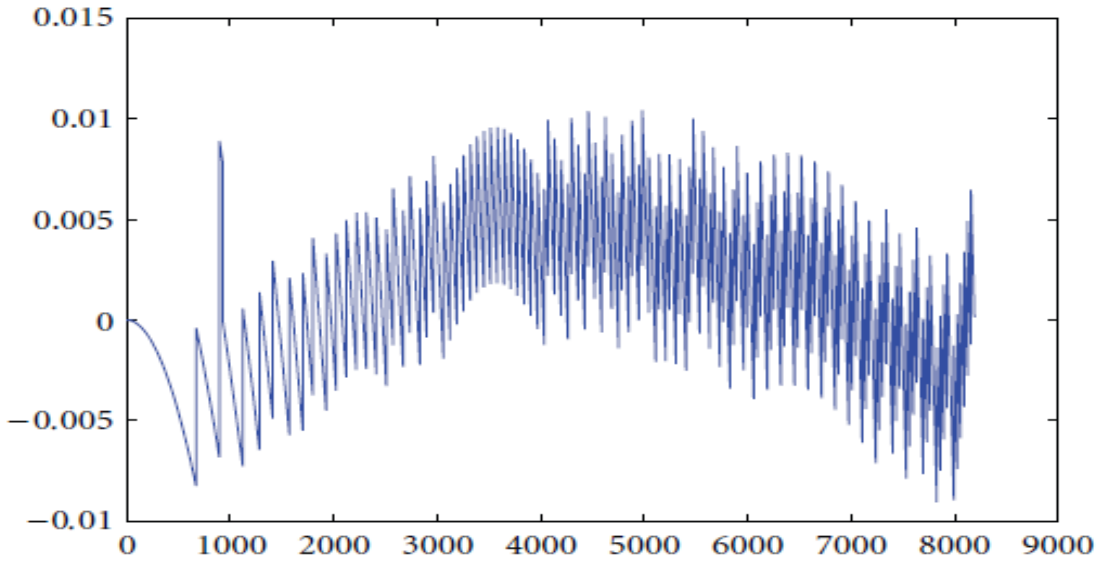

FIGURE 13: Error plot between software-generated and hardware-generated cosine wave.

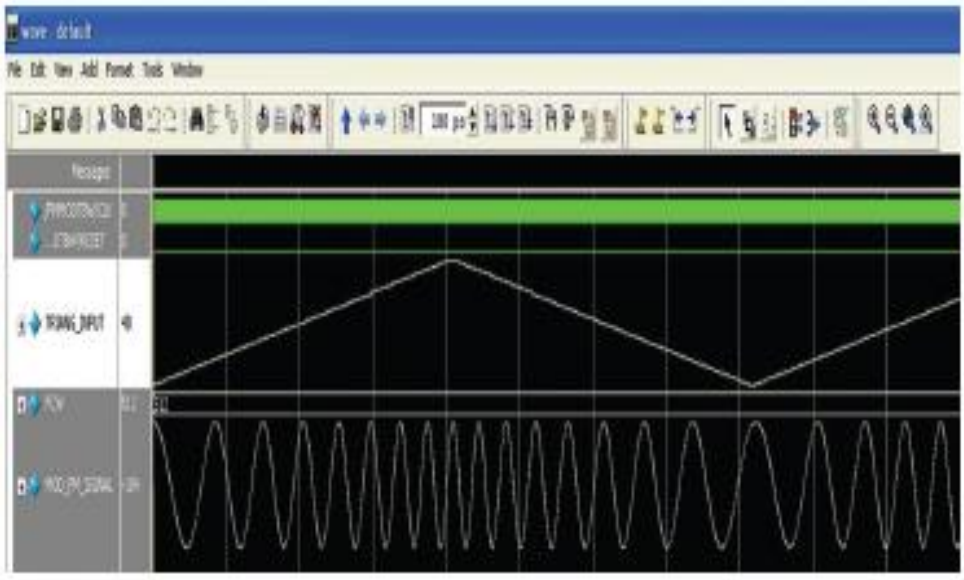

FIGURE 15: Simulation result of digital FM modulator.

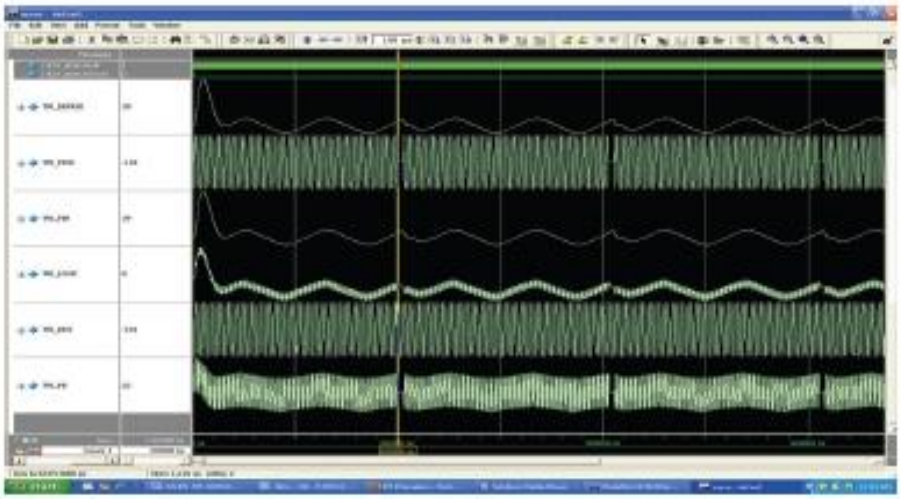

FIGURE 16: Simulation result of FM demodulator for Triangular wave modulated input.

CONCLUSIONS

A new high-performance digital FM modulator and a digital phase-locked loop-based FM demodulator have been proposed in this paper. The FM modulator and demodulator are designed to satisfy the constraint for the application in personal wireless communication and digital audio broadcasting. Individual component wise optimization has made the overall design superior than other implementations.

FPGA implementation of the proposed design has been carried out for quick prototyping of the digital FM modulator and demodulator chip. The simulation and synthesis result of FM modulator shows that the digital up conversion is very much possible as it can achieve maximum clock frequency of 334.5MHz. From the on-chip-verified result it can be clearly seen that the proposed FM demodulator can demodulate the signal back in its original form by consuming only 6.4 K equivalent gate count. The comparison results for both FPGA and ASIC implementations have shown that the proposed design is superior to the existing digital FM chips. Hence it is concluded that the designed high-performance

FM modulator and demodulator can be easily fitted into the next generation software-defined radio-based handset where low power and minimum hardware utilization with the maximum clock frequency are desired features.

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